Remarks

The purpose of this Preliminary Amendment is to conform to United States Patent and Trademark Office practice and not for the purpose of patentability. No new matter has been added by way of this Preliminary Amendment.

Respectfully submitted,

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In the Claims

1. (amended) A read write amplifier for a DRAM memory cell [(15)], which, for evaluation of the information content of at least one DRAM memory cell [(15)], is connected or can be connected to at least one bit line [(12)] and to at least one reference bit line [(13)], which in each case form a bit line pair [(16)], having a number of components for assessment, amplification and forwarding of voltage signals read from the bit lines [(12)] and reference bit lines [(13)], in which case the read/write amplifier [(30)] has a first read/write amplifier element [(40)] and a second read/write amplifier element [(50)] separate therefrom, and in that the individual amplifier components are divided between the two read/write amplifier elements [(40, 50)].

2. (amended) The read/write amplifier as claimed in claim 1, [characterized in that] wherein the amplifier components have at least one N latch circuit [(41; 51)] for amplifying a voltage signal to a low level and/or at least one P latch circuit [(42)] for amplifying a voltage signal to a high level and/or at least one equalizer [(43)] for producing a reference voltage value on the bit line(s) [(12)] and the reference bit line(s) [(13)] and/or at least one bit switch [(54)] for connecting at least one selected bit line pair [(16)] to at least one external data line [(31)].

3. (amended) The read/write amplifier as claimed in claim 2, [characterized in that] wherein at least one N latch circuit [(41)] and at least one P latch circuit [(42)] are provided in the first read/write amplifier element [(40)].

4. (amended) The read/write amplifier as claimed in claim 2 [or 3], [characterized in that] wherein at least one equalizer [(43)] is provided in the first read/write amplifier element [(40)].

5. (amended) The read/write amplifier as claimed in [one of] claim[s] 2 [to 4], [characterized in that] wherein at least one N latch circuit [(51)] is provided in the second read/write amplifier element [(50)].

6. (amended) The read/write amplifier as claimed in [one of] claim[s] 2 [to 5], [characterized in that] wherein at least one bit switch [(54)] is provided in the second read/write amplifier element [(50)].

7. (amended) The read/write amplifier as claimed in [one of] claim[s] 1 [to 6], [characterized in that] wherein the second read/write amplifier element [(50)] is connected or can be connected to at least one external data line [(31)].

8. (amended) The read/write amplifier as claimed in [one of] claim[s] 1 [to 7], [characterized in that] wherein the second read/write amplifier element [(50)] is connected or can be connected to at least one further read/write amplifier [(32)].

9. (amended) The read/write amplifier as claimed in [one of] claim[s] 1 [to 8], [characterized in that] wherein the first [(40)] and/or second [(50)] read/write amplifier element(s) has/have one or more transistors [(45; 55)] for changing over between different bit lines [(12)] and reference bit lines [(13)], respectively.

10. (amended) A DRAM memory, having a number of DRAM memory cells [(15)], which each form one or more memory cell arrays [(11)], each memory cell [(15)] being connected to a bit line [(12; 13)] and the bit lines [(12; 13)] furthermore being connected to at least one read/write amplifier [(20; 30)], [characterized in that] wherein the at least one read/write amplifier is designed as a read/write amplifier [(30)] as claimed in [one of] claim[s] 1 [to 9].

11. (amended) The DRAM memory as claimed in claim 10, [characterized in that] wherein at least one word line [(14)] is provided, which is routed across the memory cell array(s) [(11)] and, for activation of the DRAM memory cells [(15)], is connected to one or more memory cell(s) [(15)].

12. (amended) The DRAM memory as claimed in claim 10 [or 11], [characterized in that] wherein a plurality of bit lines [(12; 13)] of a memory cell array [(11)] are connected to a read/write amplifier [(30)].

13. (amended) The DRAM memory as claimed in [one of] claim[s] 10 [to 12], [characterized in that] wherein in each case a bit line [(12)] of a DRAM memory cell [(15)] that is to be evaluated and a reference bit line [(13)] of a DRAM memory cell [(15)] that is not to be evaluated form a bit line pair [(16)], and in that each bit line pair [(16)] is connected both to the first [(40)] and to the second [(50)] read/write amplifier element.

14. (amended) The DRAM memory as claimed in [one of] claim[s] 10 [to 13], [characterized in that] wherein the connection of a bit line [(12)] and/or reference bit line [(13)] to a read/write amplifier [(30)] is activated or can be activated via one or more transistors [(45; 55)].

15. (amended) A method for evaluating DRAM memory cells of a DRAM memory, in particular of a DRAM memory as claimed in [one of] claim[s] 10 [to 14], and in particular using a read/write amplifier as claimed in [one of] claim[s] 1 [to 9], having the following steps:

a) activation of one or more memory cells that are to be evaluated via at least one word line;

b) activation of a connection of at least one first bit line pair, formed from a bit line of the memory cell that is to be evaluated and a reference bit line of a memory cell that is not to be evaluated, to a first read/write amplifier element, and activation of the connection of at least one second bit line pair, adjacent to the first bit line pair, to a second read/write amplifier element, the two bit line pairs in each case being connected to the first and second read/write amplifier elements;

c) amplification of the voltage signals read out via the first bit line pair by means of at least one N latch circuit provided in the first read/write amplifier element and also a P latch circuit, and amplification of the voltage signals read out via the second bit line pair by means of at least one N latch circuit provided in the second read/write amplifier element;

d) evaluation and writing back of the data of the memory cell(s) that is/are to be evaluated and is/are actively connected to the first read/write amplifier element;

e) changeover of the connection between the bit line pairs and the first read/write amplifier element in such a way that the P latch circuit of the first read/write amplifier element is changed over to the second read/write amplifier element;

f) evaluation and writing back of the data of the memory cell(s) that is/are to be evaluated and is/are actively connected to the second read/write amplifier element; and

g) deactivation of the memory cells that are to be evaluated.

17. (amended) The method as claimed in claim 15 [or 16], [characterized in that] wherein the bit line pair which is actively connected to the first read/write amplifier element is disconnected from the first read/write amplifier element after the end of step d), with the result that the bit line and the reference bit line float with full voltage levels, and in that the N latch circuit of the first read/write amplifier element is subsequently switched off.

18. (amended) The method as claimed in [one of] claim[s] 15 [to 17], [characterized in that] wherein, after the activation of a bit switch provided in the second read/write amplifier element, a voltage difference is generated on one or more external data line(s) connected to said bit switch.

19. (amended) The method as claimed in [one of] claim[s] 15 [to 18], [characterized in that] wherein, after the end of the evaluation operation, the uniform reference voltage is applied to all the bit lines of the evaluated memory cells via an equalizer.